

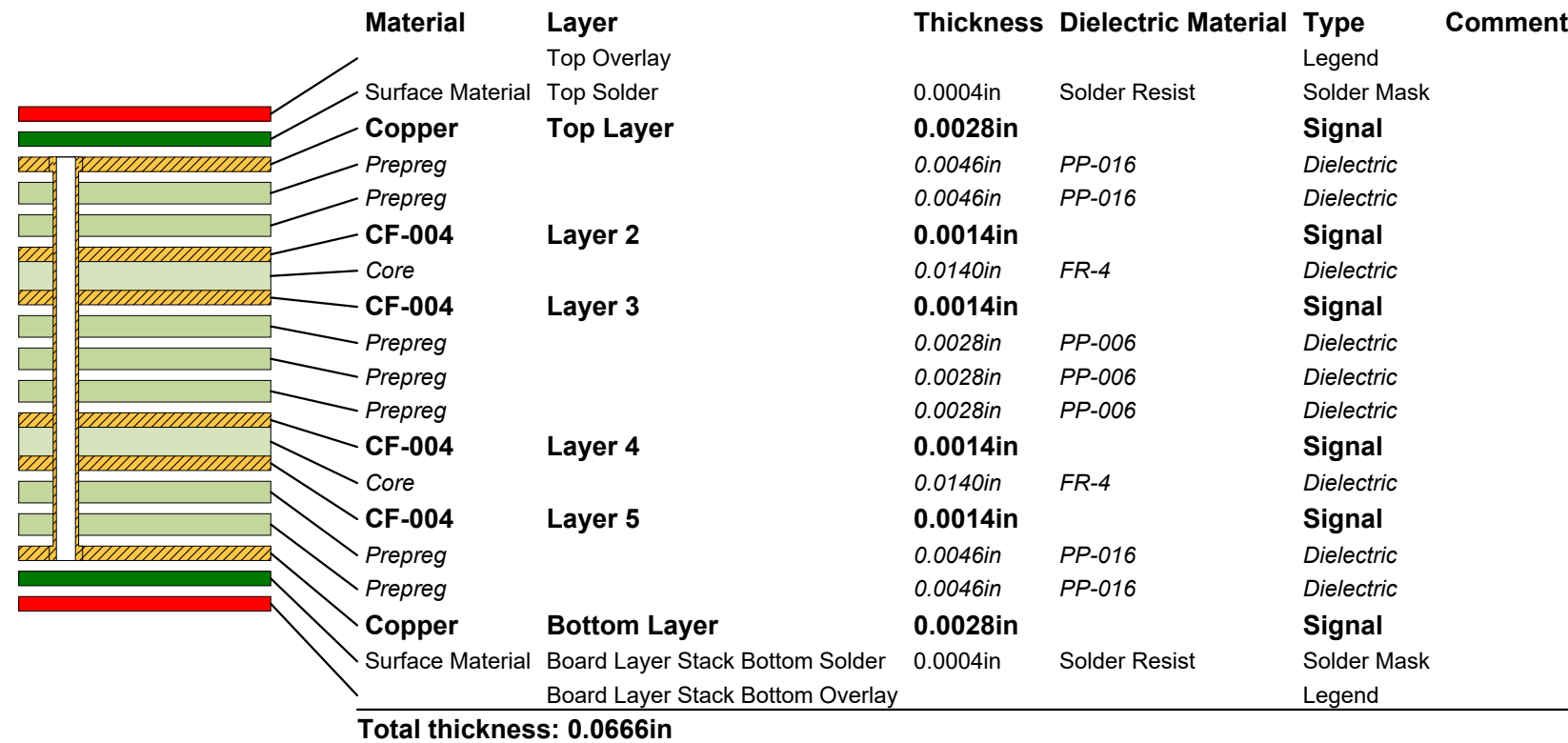
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REVISION	DESCRIPTION	DATE	APPROVED

NOTES: (UNLESS OTHERWISE SPECIFIED)

1. BOARD FABRICATION METHODS MUST COMPLY WITH:
FABRICATE IN ACCORDANCE WITH IPC-6018B, per IPC-6011, CLASS 2.
2. ARTWORK FORMAT: GERBER 274X
GERBER DATA SUPPLIED WITH DESIRED FINAL TRACE WIDTHS. PROCESS
COMPENSATION TRACE WIDTH ADJUSTMENTS TO BE DONE BY PCB FABRICATOR
3. FINISH PLATING:
METAL 1 (TOP) AND METAL 2 (BOTTOM):
ENIG (ELECTROLESS NICKEL/IMMERSION GOLD):
ELECTROLESS NICKEL per IPC-4552, 118 - 236µin. (3 - 6µm)
IMMERSION GOLD per IPC-4552, 3 - 10 µin (0.08 - 0.25µm)
4. FINISHED BOARD THICKNESS: (SEE LAYER STACK LEGEND) ± 10%
5. TOLERANCE: PC BOARD OUTLINE: ±0.003in.TOLERANCE:
A. PC BOARD OUTLINE: ±0.003in.
6. VIA PLATING/FILLING:
A. ALL OTHER PLATED THRU HOLES TO BE PLATED TO 0.0007in. MIN. THICKNESS.
7. CONDUCTOR WIDTHS AND SPACING TO BE WITHIN 0.001in. OF CAD DATABASE.
8. ALL HOLES TO BE LOCATED WITHIN ±0.003 OF CAD DATABASE.
9. THE PCB SHALL BE MARKED WITH BOTH THE FABRICATOR'S NAME OR LOGO AND A DATE CODE
SHOWING CALENDAR YEAR AND WEEK (YY/WW).
10. DELIVER BOARDS BAGGED AS: SINGLES
11. 100% ELECTRICAL TEST USING SUPPLIED IPC-D-356 NETLIST.
12. THE DELIVERED BOARDS SHALL BE LEAD-FREE AND RoHS COMPLIANT.

LAYER STACK LEGEND

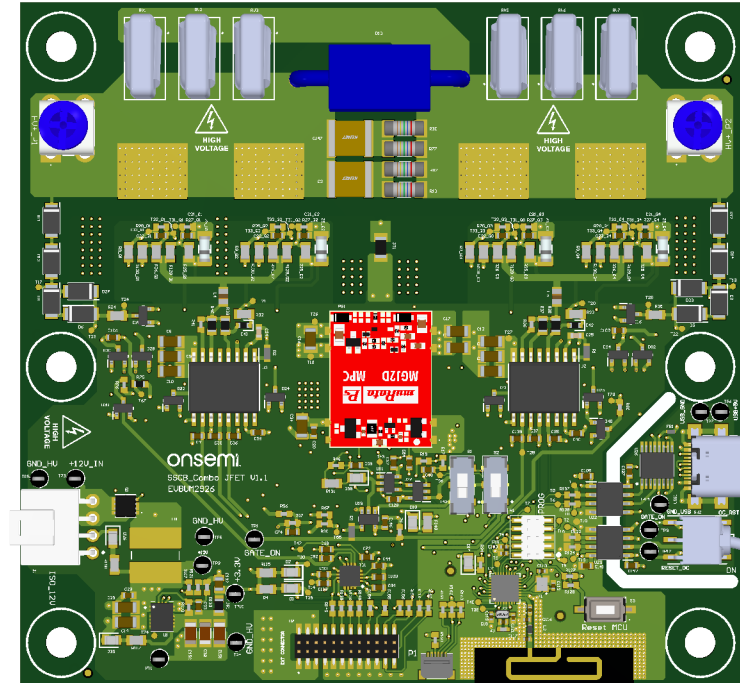


Total thickness: 0.0666in

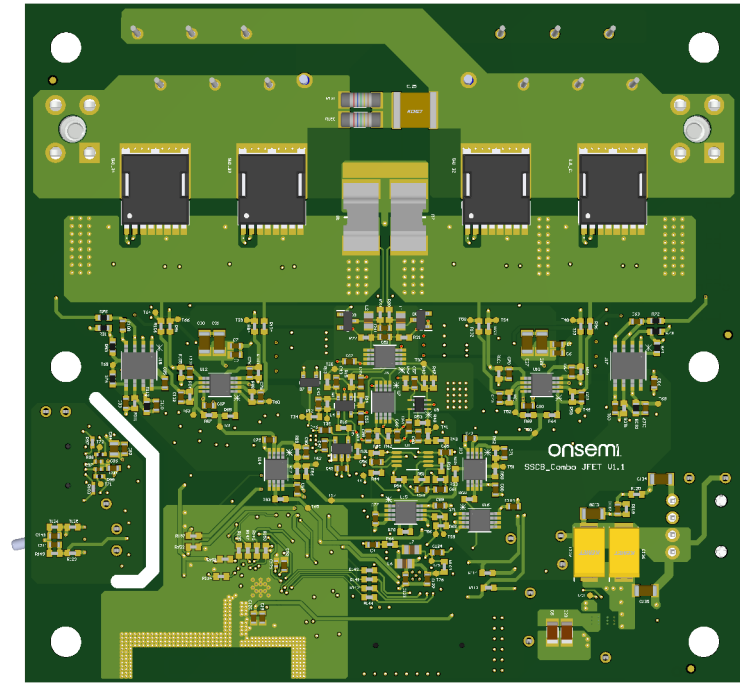
APPROVALS	DATE	PROJECT	ADDRESS 1		.ItemRevision
ENG: Shusun Qu	--/--	*	ADDRESS 2		
DSN: Shusun Qu	--/--		ADDRESS 3		
CHK: --/--			ADDRESS 4		
REFERENCE DOCUMENTS		PROJECT REVISION	DOCUMENT REVISION	DESIGN ITEM	
BOM: =DOC_NO_BOM	=VersionControl ProjNotRevisedControl				
ASSY DWG: =DOC_NO_ASSY		SSCB_Combo JFET V1.1			
FAB DWG: =DOC_NO_FAB_DWG	=CAGE_CODE =DOC_NO_SCH_DWG			.ItemRev	
PCB DWG: =PCB_DWG_NO	SCALE =SCH_FNAME =SSCB_Combo JFET V1.1			PCB dwg	OF 4

REVISION	DESCRIPTION	DATE	APPROVED

Realistic Top View



Realistic Bottom View



APPROVALS	DATE	PROJECT	onsemi	ADDRESS 1	ADDRESS 2	ADDRESS 3	ADDRESS 4
ENG: Shusun Qu	--/--	*					
DSN: Shusun Qu	--/--	PROJECT REVISION	DOCUMENT REVISION	DESIGN ITEM			
CHK: --/--	--/--	TITLE	SSCB_Combo JFET V1.1				
REFERENCE DOCUMENTS							
BOM: =DOC_NO_BOM							
ASSY DWG: =DOC_NO_ASSY_DWG							
FAB DWG: =DOC_NO_FAB_DWG							
PCB DWG: =PCB_DWG_NO							